Comparison of on-wafer calibrations for measurements of active and passive devices at millimeter-wave frequencies

Sang-Hee Shin[1] | Nick Ridler[1] | Andrew Tucker[2] | Tudor Williams[2] | Xiaobang Shang[1]

[1]National Physical Laboratory, Electromagnetic & Electrochemical Technologies Department, Teddington, TW11 0LW, U.K.

[2]Filtronic, Plexus 1, NET Park Thomas Wright Way, Sedgefield, Country Durham, TS21 3FD, UK.

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Abstract

In this paper, we present the measurement of active and passive on-wafer devices, at W-band (75-110 GHz), using five conventional calibration schemes: Short-Open-Load-Thru (SOLT), Thru-Reflect-Line (TRL), multiline TRL (MTRL), Line-Reflect-Match (LRM), and Line-Reflect-Reflect-Match (LRRM). Generally, measurement results with respect to different calibration methods show relatively good agreement. The results deviate slightly from each other due to factors such as the choice of line standards for TRL and the imperfect definition of matched load standards for SOLT, LRM, and LRRM schemes, etc. Differences in the results are quantified and discussed. This comparison provides quantitative information about the performance of different calibration schemes at millimeter-wave frequencies and can facilitate the choice of calibration methods by other users, which will benefit the on-going development of passive and active planar circuits used at these frequencies.

Keywords

on-wafer measurement, calibration, mm-wave, vector network analyzer, transistor, S-parameters

1 | INTRODUCTION

On-wafer S-parameter measurement underpins the development of millimeter-wave (mm-wave) passive and active devices and circuits[1,2]. Therefore, there has been an increasing interest in the development of accurate calibration and de-embedding techniques, such as those reported in[3-6]. On-wafer calibration allows devices under test (DUTs) and calibration standards to have nominally the same substrates, fabrication processes and boundary conditions. Therefore, unlike off-wafer calibration, which uses a separate commercial calibration substrate, on-wafer calibration does not require subsequent processes for removing parasitic effects associated with probe-substrate interactions. A study on off-wafer calibrations of an active device using commercial calibration substrates has shown that the pad parasitic and dielectric constant differences between the calibration substrate and DUT substrate cause inaccurate calibrations[7]. Studies have also shown that on-wafer calibrations provide superior accuracies compared to off-wafer calibrations[8,9]. Therefore, in this work, only on-wafer calibrations are considered.

There exist different calibration schemes and among them, the most popular ones include Short-Open-Load-Thru (SOLT)[10], Thru-Reflect-Line (TRL)[11], multiline TRL (MTRL)[12], Line-Reflect-Match (LRM)[13], and Line-Reflect-Reflect-Match (LRRM)[14]. Such calibration methods have shown relatively good agreement at frequencies below 10 GHz[15]. However, in the mm-wave frequency range, the calibration schemes show significant differences in measurement results[7,16]. On-wafer measurements at mm-wave frequencies inherently suffer from error-inducing factors such as inconsistent probe landing, fabrication tolerances, coupling between adjacent neighboring structures, propagation of unwanted modes, probe-substrate parasitic effects, etc. In addition, crosstalk between the probes is known to have a significant effect on on-wafer measurements[17]. The choice of calibration method tends to produce different measurement results, in that some calibration schemes can tolerate these error-inducing effects better than others.

For example, the SOLT calibration scheme requires all standards to be accurately defined[18]. The SOLT scheme uses fixed definitions for standards, for a perfect probe placement scenario; hence it is highly sensitive to errors due to imperfect probe landing. In addition, the SOLT scheme requires the calibration standards to be manufactured with a high fabrication accuracy[13]. Typically, at mm-wave frequencies, the impact of the fabrication accuracy increases, and this can cause the reliability of the SOLT calibration to be compromised.

The TRL calibration scheme does not require all the standards to be accurately defined. The Reflect standards (e.g., Open or Short) do not need to be well defined but must be identical for each port[19]. It also benefits from the line standard having a phase delay of typically between 30° to 150°, across the frequency range. As a result, the TRL scheme with a single line standard is inherently band limited. MTRL uses a combination of multiple lines with varying lengths[12]. Since it uses a weighted average of the line measurements, it can resolve the conventional TRL

scheme's band limitation issue with an appropriate selection of lines. The reference impedance for both TRL and MTRL schemes is determined according to the characteristic impedance of the line standards.

The LRM and LRRM calibration schemes do not require every standard to be accurately defined[14]. However, they require identical reflect standards for each port. For the LRM calibration scheme two accurately defined match standards are required for two-port measurements, whereas the LRRM scheme only requires one. Also, the LRRM scheme utilizes two pairs of reflecting standards (typically shorts and opens), while the LRM scheme only uses a single pair (either shorts or opens). The LRM and LRRM schemes are not band limited.

Despite the widespread use of these five conventional calibration techniques, a comprehensive comparison of these methods using state-of-the-art circuits up to 110 GHz has not yet been reported. Here, we have compared these calibration schemes, at W-band (75-110 GHz), using both the latest developed active devices (transistors fabricated based on WIN Semiconductors GaAs pHEMT process PP10-20) and conventional passive devices (transmission lines and loads on a commercial impedance standard substrate, CS-5 from GGB[20]) as the DUTs. By comparing the measured S-parameters of these DUTs, corrected using various calibration schemes, the differences between each calibration scheme have been quantified and are subsequently discussed. This can facilitate the selection of desired calibration techniques and is essential for the accurate and consistent characterization of mm-wave planar circuits.

The paper is organized as follows. In Section 2, the calibration standards used for both the active and passive device measurements are discussed. Following the description of the measurement results in Section 3, an in-depth discussion is provided in Section 4, and a conclusion is given in Section 5.

2 | CALIBRATION STANDARDS

2.1 | Active Devices

Four different calibration schemes are employed for the transistor measurements: TRL, MTRL, LRM, and LRRM. Since accurate definitions of each calibration standard are not available, the SOLT scheme was not used in this case. The calibration standards are fabricated on the same GaAs substrate as the DUT transistor using an identical manufacturing process. The calibration reference planes are at the center of the thru standard, as shown in Figure 1 (a). Examples of the standards and the DUT transistor used for the measurements are shown in Figure 1.

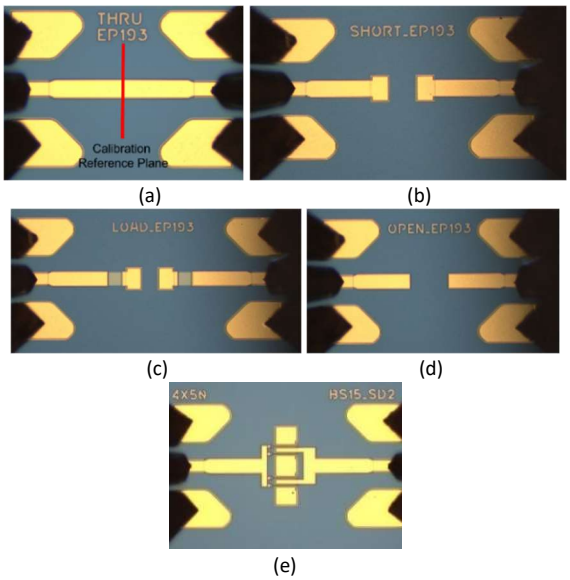
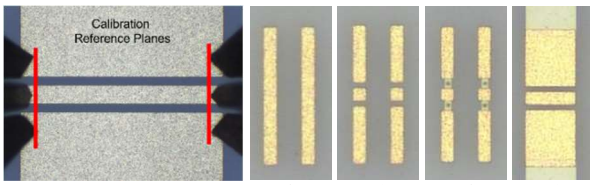


Figure 1 Microscope images of on-wafer calibration standards for active DUT measurements: (a)Thru standard showing the calibration reference plane; (b) Reflect standard (short); (c) match; and (d) Reflect standard (open); (e) DUT transistor

Only two on-wafer line standards, 400 µm and 600 µm, were available for the transistor measurements. Although the 400 µm line can cover the W-band frequency range, it does not provide optimal performance. Ideally, a line standard with 90° phase delay at the center of the band should be used for the conventional single-line TRL calibration scheme. Therefore, it is possible to predict that with the current set-up, accuracy of the single-line TRL calibration scheme will degrade at the higher frequency range as the effective phase delay approaches the 150° threshold. With the MTRL scheme, using the additional 600 µm line is expected to give a more accurate calibration at the higher frequency range. Note that a generic permittivity of 12.9 was used to estimate the phase delay.

2.2 | Passive Devices

With the CS-5 impedance standard substrate (ISS), the calibration standards' definitions are utilized, since we use probes provided by the same manufacturer (GGB). Therefore, the SOLT calibration scheme is also possible. For these measurements, five different calibration schemes are employed: TRL, MTRL, SOLT, LRM, and LRRM. Both DUTs and the calibration standards are on the same ISS (with alumina substrate). The calibration reference planes are at the tip of the probes, as shown in Figure 2(a). Examples of the calibration standards used for the passive DUT measurements are shown in Figure 2.



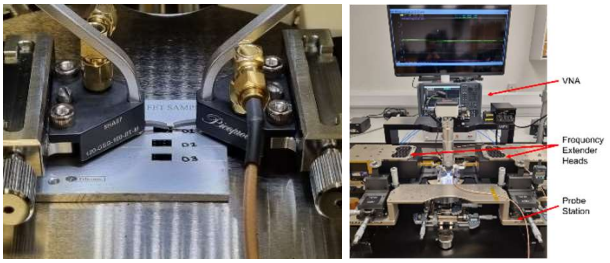
(a) (b) (c) (d) (e)

Figure 2 Microscope images of the ISS calibration standards used for the passive DUT measurements: (a) calibration reference plane (at the probe-tips); (b) shorts; (c) opens; (d) loads; and (e) thru.

3 | MEASUREMENT COMPARISON

3.1 | Measurement Set-up

All the measurements were conducted using an MPI TS150-THZ probe station, Keysight PNA-X vector network analyzer (VNA), VDI W-band frequency extender heads, and a pair of GGB 100 µm pitch GSG probes (120-GSG-100-BT-M). The measurement setup is shown in Figure 3.



(a) (b)

Figure 3 Photograph of the measurement set-up; (a) close-up view of the landed probes; (b) setup overview, showing the probe station, VNA, and frequency extender heads.

For both transistor and ISS measurements, uncalibrated (raw) measurement data was recorded for each calibration standard and DUT and corrections (i.e. calibrations) were implemented off-line. This minimizes the impact due to errors associated with system drift and inconsistent probe landing. After collecting all the raw data, off-line calibrations were employed using WinCal XE 4.9[21]. For the TRL and MTRL calibration schemes, the corrected results were re-normalized to 50 Ω, using the well-known methods[22, 23]. In addition to the measured DC load resistance, a load inductance value provided by the manufacturer was also used.

A metal chuck was used for the transistor measurement, since the microstrip structures already have a ground plane on the bottom surface of the substrate. With the CS-5 substrate, since the DUTs and calibration standards are based on co-planar waveguide (CPW), without a conductor layer at the bottom surface, a ceramic chuck was used to reduce the effect of any unwanted modes[24].

3.2 | Transistor Measurement

For the active device measurements, a 0.1 µm GaAs pHEMT transistor with 4 gate fingers (50 µm width) was used as the DUT. The gate (0.02 V) and drain (3.5 V) bias was applied to the transistor using the built-in bias tees of the probes.

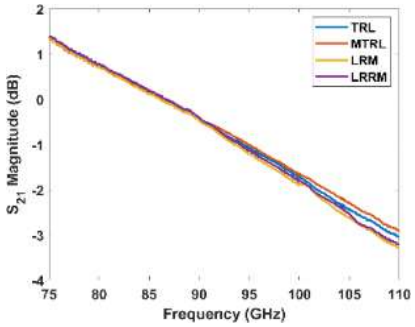


Figure 4 On-wafer calibration comparison of an active transistor device.

Figure 4 shows the $|S_{21}|$ measurement of the transistor with respect to the four different calibration schemes (normalized to 50 Ω): TRL, MTRL, LRM, and LRRM. At the lower frequency range (i.e. 75 to 90 GHz), the calibrated results are nearly identical to each other. However, a clear deviation (up to 0.4 dB) between TRL/MTRL and LRM/LRRM schemes can be observed at the higher frequency range (i.e., above 100 GHz). The difference increases with the frequency.

3.3 | Impedance Standard Substrate CS-5 Measurement

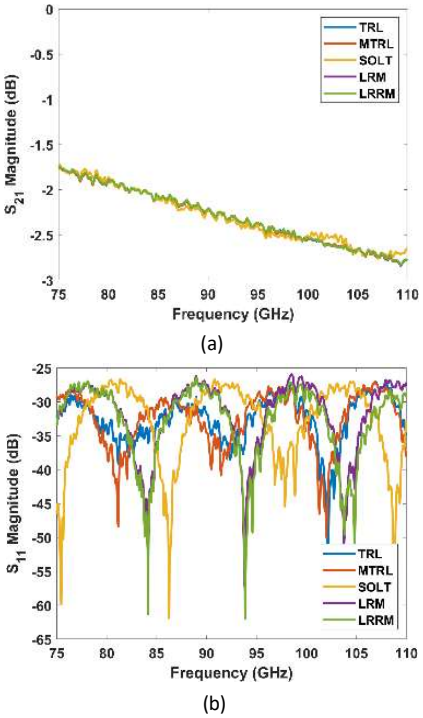


Figure 5 On-wafer calibration comparison of a CPW line on CS-5 ISS; (a) S_{21} magnitude, (b) S_{11} magnitude.

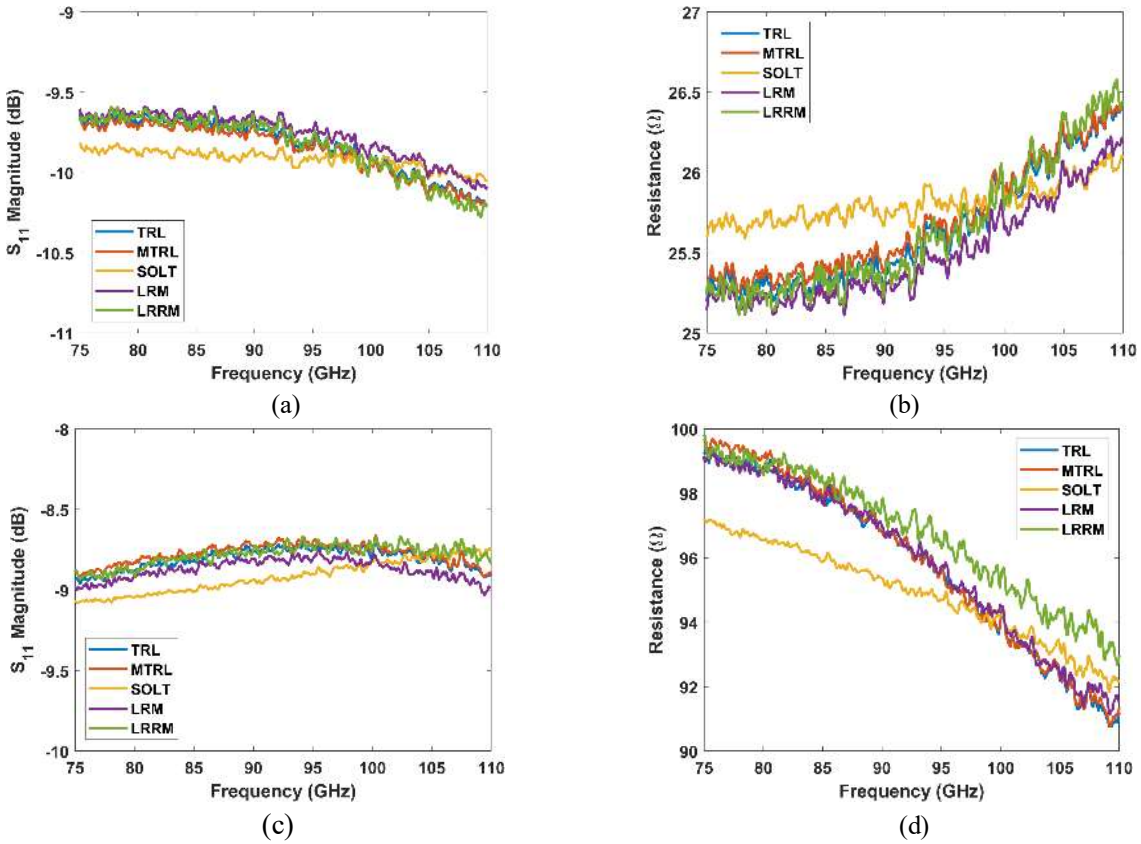


Figure 6 On-wafer calibration comparison of a 25 Ω and 100 Ω load on CS-5 ISS: (a) S_{11} magnitude (25 Ω); (b) extracted equivalent resistance (25 Ω); (c) S_{11} magnitude (100 Ω); (d) extracted equivalent resistance (100 Ω)

Figure 5 (a) shows $|S_{21}|$ measurements of a 6532 µm (measured probe tip-to-tip distance) line on the CS-5 ISS, calibrated with the following calibration schemes (normalized to 50 Ω): TRL, MTRL, SOLT, LRM, and LRRM. For the transmission measurements, calibrated results from the TRL, MTRL, LRM, and LRRM calibration schemes show very good agreement across W-band. The SOLT calibrated results show a noticeable deviation across the frequency band. The deviation is more significant at the higher frequency range (above 100 GHz).

Figure 5 (b) shows the measured $|S_{11}|$ results of the measured CPW line. All the results show ripples with a consistent peak to trough distance $\Delta f \approx 5$ GHz. The calculated distance between two mismatch planes is $d = c/(4\Delta f\sqrt{\epsilon_{eff}}) \approx 6600\mu m$, where ϵ_{eff} is the effective permittivity of the CPW line and c is the speed of light. This is approximately the measured distance between port 1 and 2 probe contact points, suggesting that the mismatch behaviour seen in the measurement results is likely to be due to mismatches caused by the probe contact points. In terms of peak return loss, the TRL and MTRL results show very good agreement with each other. The LRM and LRRM results show near-perfect agreement with each other but slightly higher peak return loss than the TRL and MTRL results. The SOLT result show

s a similar return loss level as the LRM and LRRM results, albeit at slightly different frequencies.

Figure 6 (a) shows the S_{11} result of a 25 Ω load on the CS-5 ISS, calibrated using the same five calibration schemes (normalized to 50 Ω). It can be seen that at the lower frequency range (below 90 GHz), all the calibrated results, except SOLT, show good agreement. Above 90 GHz, the LRM calibrated result shows a slight deviation of up to ~ 0.1 dB.

Figure 6 (b) shows the equivalent measured resistance of the 25 Ω (nominal) load, derived from the S_{11} measurements; $R_{load} = Re(Z_{ref}(1 + S_{11})/(1 - S_{11}))$, where Re denotes real part of a complex number and Z_{ref} is the reference impedance (50 Ω). All the calibration schemes show good agreement at the lower frequency range (below 90 GHz), with the exception of the SOLT scheme. At the higher frequency range, the LRM scheme shows slight deviation up to ~ 0.2 Ω. It can also be seen that, for all the calibration schemes, as the frequency increases, the difference between nominal and measured resistance increases.

Figure 6 (c) shows the $|S_{11}|$ measurement of a 100 Ω load on the CS-5 ISS, calibrated with the same five calibration schemes (normalized to 50 Ω). The results show that at frequencies below 100 GHz, the TRL, MTRL, and LRRM schemes show good agreement. However, the LRM calibrated results show a -0.05 to -0.1 dB offset, across the

whole band. In addition, at the higher frequency range (i.e., above 100 GHz), the LRRM calibrated results start to diverge from the TRL and MTRL results. As with previous results, SOLT calibrated results show poor agreement with the other calibration schemes.

Figure 6 (d) shows the equivalent measured resistance of the 100 Ω (nominal) load, derived from the S_{11} measurements. The results indicate that all the calibration schemes show good agreement at the lower frequency range, except for the SOLT scheme. However, the LRRM calibration scheme starts to diverge above around 85 GHz. It is important to note that the discrepancy between S_{11} magnitude ($|S_{11}|$) and extracted resistance (R_{load}) exists due to the conversion process involving divisions of complex numbers. Like the 25 Ω load results, as the frequency increases, the difference between nominal and measured resistance increases.

4 | DISCUSSION

For active device transmission measurements, we have seen that, as the frequency increases, the result from each calibration diverges. As mentioned in Section 2, we expect the accuracy of the TRL calibration to degrade at the higher frequencies, because the length of the line standard is not optimal at these frequencies. We expect that the MTRL calibrated result to be more reliable because it utilizes an additional line with a suitable effective phase delay at the higher frequency range. With LRM and LRRM results, even more deviation from the MTRL result can be observed. This is likely due to the LRM and LRRM schemes assuming the resistance and inductance of the matched load standard to be fixed values, independent of frequency.

The passive measurements, like the transistor measurements using TRL, MTRL, LRM and LRRM calibration schemes, show good agreement at the lower frequency range. In addition, the TRL and MTRL calibrated results are nearly identical across the entire W-band. As the line standard used for the TRL calibration scheme already has near-optimal effective phase delay, using additional lines for the MTRL scheme does not show significant improvement.

With the ISS calibrations and measurements, the SOLT calibration scheme was also employed. The DUT line measurement results clearly show that SOLT does not perform well at higher frequencies. Moreover, the 25 Ω and 100 Ω load measured results indicate that even at the lower-end of W-band frequency range, SOLT calibrated results show poor agreement when compared to the other calibration schemes. This suggests that the nominal definitions of the calibration standards used for the SOLT scheme, are not sufficiently accurate for these measurements, as factors such as probe and ISS condition, as well as landing positions, are not perfect.

5 | CONCLUSION

In this paper, we compared five calibration schemes that are commonly used during on-wafer measurement at W-band. Both active and passive devices were measured with respect to the following calibration schemes: TRL, MTRL, LRM, and LRRM. For passive devices, an additional SOLT scheme was employed. It was found that TRL, MTRL, LRM, and LRRM measurement schemes generally showed good agreement for measurements of both passive and active devices. However, at the higher frequency range, we were able to observe that, due to the sub-optimal choice of the line standards for TRL (for the transistor DUT) and with a fixed definition of the matched load standard for LRM and LRRM, the calibrated results started to diverge. With SOLT calibration, the calibrated results showed significant differences when compared to the other calibration schemes. The differences are likely due to the SOLT scheme being particularly sensitive to the accuracy of the calibration standards' definition.

It is difficult to have calibration standards with accurate definitions for on-wafer measurements. Therefore, calibration schemes such as TRL and MTRL that require the least knowledge of the calibration standards are expected to produce more reliable and consistent results. Here we have shown that the choice of calibration scheme can significantly impact the measurement results. This work has also shown that, even with the calibration definitions provided by the substrate and the probe manufacturer, the SOLT scheme's accuracy and consistency might not be sufficient. It is clear that identifying and recognizing these differences is necessary for choosing an application-appropriate calibration scheme and, for understanding and interpreting the results.

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