A Template for Doherty Amplifier Design

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Abstract

The Doherty architecture of RF Power Amplifiers has been studied extensively since its initial conception in 1936, however it remains challenging for a designer to identify and monitor the numerous interactions of passive and active components as a design moves from ideal concept to manufacturable circuit. This work enumerates a set of key performance indicators specific to the Doherty architecture and presents measurement and display techniques to analyze them at all design stages. The approach is demonstrated up to manufacturing using the Keysight PathWave Advanced Design System software, following step-by-step a case study design of a compact Doherty Power Amplifier for 5G MIMO applications.

1 Introduction

Modern wireless communications schemes use complex modulations with large amplitude dynamic in order to achieve higher data rates and use more efficiently the limited spectral resources. For mobile base stations, Orthogonal Frequency Division Mutiplexing is the current standard, that results in waveforms with typical Peak to Average Power Ratios (PAPR) of around 8.5 dB for 4G LTE and up to 14 dB for 5G.

Unfortunately, this direction for increasing spectral efficiency leads to problems in terms of energy efficiency. The energy consumption in most wireless high frequency front-ends is dominated by the Power Amplifier (PA) which maximizes its efficiency when operated near saturation. However, the PA cannot be operated with a carrier power too close to saturation to avoid excessive distortion due to compression or clipping of the signal. Therefore, an output power back-off (OBO) is applied to achieve good enough linearity. This means that a standard linear PA will operate with low efficiency.

To overcome this linearity vs. efficiency trade-off, several solutions have been proposed. First of all, at signal level, crest reduction factors are applied most of the times, and the PAPR numbers indicated to PA designers usually take these into account already. Hence, they do not improve the situation for the PA but at least they eliminate very large peaks that might damage the PA or create unnecessary distortion. At PA level, the most studied solutions are the Doherty PA [1, 3], the current *de-facto* standard in mobile base-stations, the Chireix Outphasing [5], and Envelope tracking [4]. The Chireix and Envelope tracking require significant changes to the architecture therefore can be seen more as trasmitter solutions rather than PA solution. On the other hand, the success of the Doherty is that it is a PA solution requiring minimal change to the transmitter architecture compared to a standard, linear PA. The more recently introduced Load Modulated Balanced Amplifier [6] offers more flexibility in terms of use of load modulation compared to the Doherty PA, but it is fundamentally based on the same concept of load modulation.

This paper will discuss the basic theory of the Doherty PA in relation to how it can be used as a starting point as a reference for a complete Doherty PA design, and how an ADS template can be used to facilitate this process.

2 Ideal Doherty PA operation

The fundamental reason for which standard linear PAs have poor efficiency at large OBO is because their output voltage does not reach the maximum span. While the output current waveform is usually rectified (class B or AB operation), the output voltage is not. Therefore, when reducing the input drive, while the current RF component reduces alongside its DC component, the voltage RF components also reduced but with a fixed DC component. Hence, the efficiency reduces when reducing the input drive. To restore efficiency, one option is to increase the RF load as the input drive reduces, therefore restoring the RF voltage swing and therefore restoring efficiency. The Doherty PA achieve this by means of active load modulation, by increasing the RF impedance to maintain a constant voltage over a certain range of input drive, corresponding to the target OBO.

Load modulation is a technique which dynamically adjusts the impedance at the output of the main transistor of the Doherty amplifier to optimize its efficiency. Two currents flowing into a common load, shown in Figure 1, will alter the perceived value of that load from the perspective of the source of each current. The magnitude and relative phases of these currents, and the effective loads which result from them are key properties to monitor.

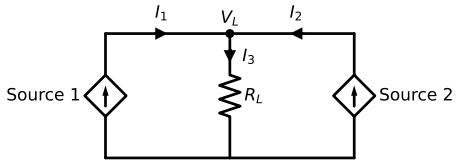


Figure 1: Two current sources modulating the effective impedance of a shared load

$$V_L = R_L(I_1 + I_2) \tag{1}$$

From the perspective of the first current generator, the voltage across the load is increasing without the first current generator's output changing. This effect is as if the value of the load were increasing to a new value R'_L. Combined with the previous result of Kirchoff's current law, the effective load of the first current generator can be expressed as:

$$\begin{aligned} R'_L &= \frac{V_L}{I_L} \\ &= \frac{R_L(I_1 + I_2)}{I_1} \end{aligned} \tag{2}$$

For the second current generator, the effect is identical though referenced to the current from the first generator. In the Doherty these generators are the Main and Auxiliary transistors.

$$R"_L = \frac{R_L(I_1 + I_2)}{I_2} \tag{3}$$

The active load modulation will become useful and relevant when the currents from the two generators are in a non-linear relationship. In the Doherty PA, the first current generator is referred as Main and represents a linear response vs. input, while the second generator, called Auxiliary, has a "threshold" behaviour with current increasing linearly only after a certain input drive threshold is achieved.

To complete the Doherty architecture, the "direction" of the load modulation must be adjusted by means of an impedance inverter positioned between the first current source and the common load, see Figure 2.

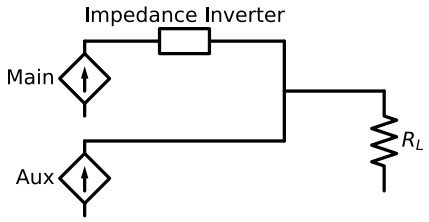


Figure 2: Block diagram of an ideal classic Doherty

It is reasonable to assume that the output power will increase when the second generator contributes to the common load current. However, the desired behaviour is for the impedance to decrease when the output power decreases, while (2) shows the opposite. Therefore, by inserting an impedance inverter, the increasing common node impedance is transformed to a decreasing main impedance when the auxiliary generator contributes. An impedance transformation network is generally used from the external 50 Ω termination to the common node impedance.

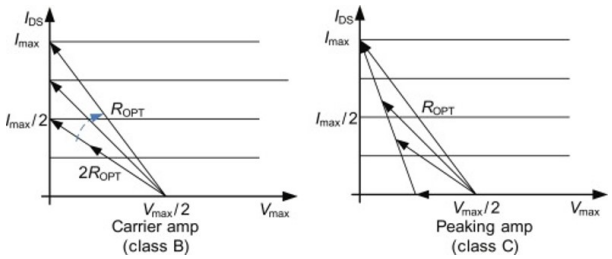


Figure 3: Loadlines for the Main and Auxiliary Transistors

3 Case-study

To illustrate the use of the design process and template, a PA targeting a 5G C-band system has been used. The specifications are to operate between 3.4-3.8 GHz, $P_{out,max}$ >40 Watts, a gain of 10 dB, and to work with a PAPR of 8.5 dB.

3.1 Initial Device Requirements

Matching the Doherty back-off point to the PAPR specification provides a useful efficiency maximum at the average power level of the waveform. Hence, by knowing the target OBO, it is possible to calculate, in first approximation, the ratio of the output power that the two active devices must provide at saturation. By definition:

$$OBO = \frac{P_{\mathrm{MAX,DPA}}}{P_{\mathrm{OBO,DPA}}} \tag{4}$$

However, at the back-off, only the main amplifier operates, so:

$$P_{\text{OBO,DPA}} = P_{\text{OBO,MAIN}} \tag{5}$$

Since the voltage of the main PA is kept constant between the back-off point and saturation, the output power of the main only increases because of the current contribution, therefore following a square-root response:

$$P_{\text{MAX,MAIN}} = \sqrt{OBO} P_{\text{OBO,MAIN}} \tag{6}$$

that means

$$P_{\text{MAX,DPA}} = \sqrt{OBO} P_{\text{MAX,MAIN}} = P_{\text{MAX,MAIN}} + P_{\text{MAX,AUX}} \tag{7}$$

therefore we can relate the power of the two devices:

$$\frac{P_{\text{MAX,AUX}}}{P_{\text{MAX,MAIN}}} = \sqrt{OBO} - 1. \tag{8}$$

Figure 4 plots the equation in (8) up to OBO of 14 dB. For obtaining exactly 8.5 dB of OBO, the power

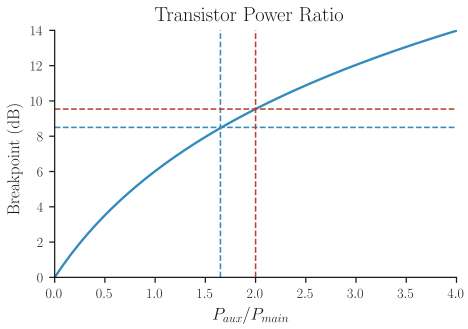


Figure 4: The PAPR goal maps to transistor power selection

ratio of the devices is $\simeq 1.7$ which is difficult to obtain with a selection of off-the-shelf components. On the other hand, a ratio of 2 is much more common, and should lead to a conservative OBO of $\simeq 9.5$ dB. Considering the target output power in excess of 40 W, the selection of the devices have converged to Wolfspeed die transistors with nominal output power of 15 W (CG2H80015D) and 30 W (CG2H80030D). Since the expected maximum voltage on these two devices is the same, the maximum currents are therefore in a 2:1 relation also, meaning that the common load will be modulated of 3:1 on the main side and 1.5:1 on the auxiliary side.

The optimum intrinsic load impedance of the devices can be estimated as:

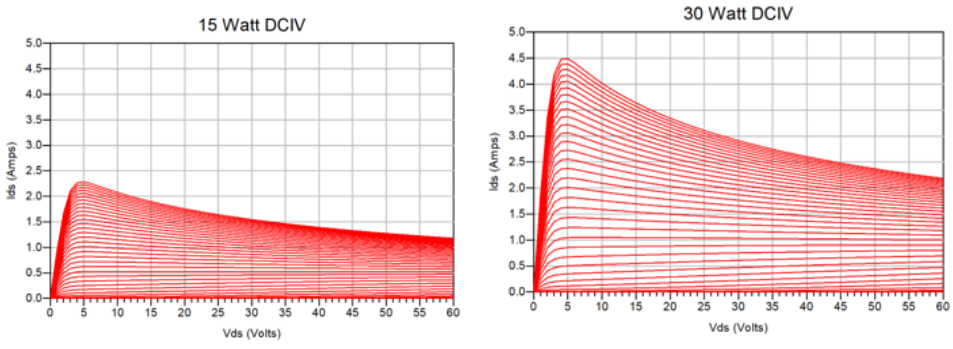
$$R_{opt} = \frac{2(V_{DD} - V_{knee})}{I_{max}} \tag{9}$$

where V_{DD} is the drain bias voltage, V_{knee} is the knee voltage and I_{max} the maximum device current. For each device, these value can be read from the DCIV simulations of the devices, see Figure 5a and 5b, leading to the results of Table 1. There is now enough information to start running a basic AC simulation

	CG2H80015D	CG2H80030D
I_{max}	2.28 Amps	4.49 Amps
V_{knee}	4 Volts	4 Volts
R_{opt}	21.2 Ohms	10.7 Ohms

Table 1: Static approximation characteristics of the devices chosen for Main and Auxiliary stages.

with ideal current sources that shows how the ideal load modulation will work in a perfect Doherty that used these devices to target the specified OBO. See Figure 6 that shows the simulation template and Figure 7 for the load modulation at the main and auxiliary devices.



(a) CG2H80015D (b) CG2H80030D

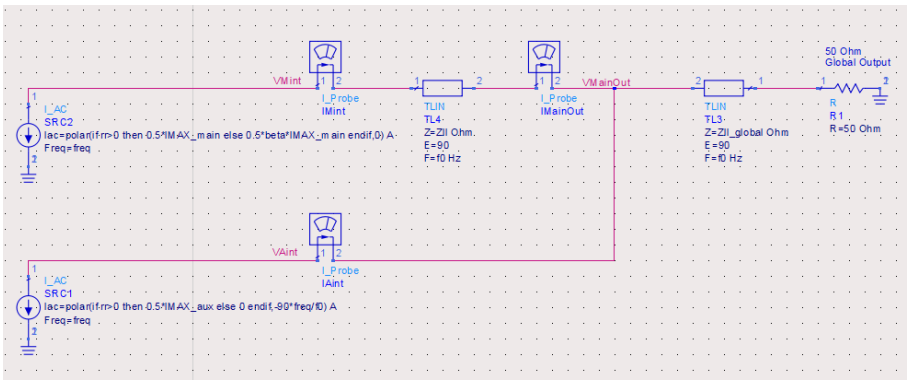


Figure 6: AC schematic of an ideal Doherty

3.2 Parasitics

The main difficulty in high frequency power amplifier design is having to deal with reactive and parasitic effects of the transistors that must be compensated for to avoid losing output power and efficiency, and that in general will limit the achievable bandwidth of the design.

Having chosen die devices instead of packaged ones gives more control in terms of controlling the parasitics of the interconnection between device and the microstrip networks, but still it does not allow to cancel them completely. In particular, the drain and gate device pads will need to be connected to the microstrip by means of bond wires.

A 3D FEM simulation has been performed to predict the 2-port passive network that represents this connection, which results in a dominant, equivalent inductance at the design frequency band. With the goal of minimizing this inductance, the active device will be placed witin a PCB recess as close as possible to the PCB walls, and die attached directly to the underlying metal carrier. The maximum number of bond wires that can be fit on the device pads has been used. The equivalent inductance L_{BW} for the two devices' launchers has been estimated as 0.22 nH for the Main, and 0.31 nH for the Auxiliary.

The dominant reactive effect at the output of a transistor, however, is capacitive, and related to the drain-to-source and drain-to-gate capacitance. For PA design purposes, it is better to consider the output capacitance as a behavioural capacitive response rather than relate it directly to physical capacitance within the device. To do so, the optimum power load vs. frequency can be analysed to see if it can be approximated with an admittance with constant conductance $(1/R_{OPT})$ and negative susceptance proportional to frequency, which means the perfect compensation for an equivalent output capacitance C_{OUT}. This value has been estimated at 1.35 pF for the main device, and 2.4 pF for the auxiliary device.

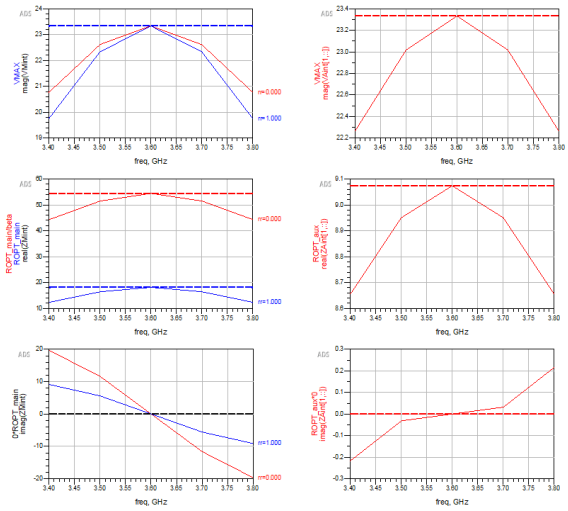


Figure 7: AC simulation of an ideal Doherty

3.3 Main Amplifier

In order to achieve a compact layout, one option for approaching the Doherty design is to use the Main matching network directly as the Doherty impedance inverter. While the most common way of realizing impedance inverters in Doherty PAs is by quarter wave transmission lines, an impedance inverter can be realized also by lumped components, and the equivalent output capacitance and inductance of the device can be part of the lumped impedance inverter. Topologically, the output of the device looks like a low-pass filter, with a shunt C_{OUT} and a series L_{BW}. This could be completed by another series inductance L_{ADD} and another shunt capacitance C_{OUT} to create a symmetrical low-pass Π network. This network will behave as a perfect impedance inverter of equivalent characteristic impedance Z_0 at frequency ω_0 if all the three branch impedance have value $|Z_0|$. Therefore, by choosing

$$Z_0 = -X_{C_{OUT}} = \frac{1}{\omega_0 C_{OUT}} \tag{10}$$

we can complete an impedance inverted by imposing:

$$L_{OUT} = L_{BW} + L_{ADD} = \frac{Z_0}{\omega_0} \tag{11}$$

Having imposed an impedance inverter with Z_0, and by knowing the impedance at back-off is $Z_{OBO,MAIN} = 3R_{OPT,MAIN} = 63.6\,\Omega$, the common node impedance can be determined:

$$Z_{CN} = \frac{Z_0^2}{Z_{OBO,MAIN}} = 14.62\,\Omega \tag{12}$$

A two stage quarterwave matching is chosen to transform the external $50\,\Omega$ to Z_{CN}.

3.4 Auxiliary

Since the common node impedance is now forced by the output capacitance of the main, the auxiliary device cannot be connected directly at the common node because the impedance observed by the main device will not be the optimum one. The option chosen has been to use the approach as for the main,

i.e., to use the output capacitance of the device to build a lumped impedance inverter, in this case of equivalent impedance of $Z_{0,A} = 16.37\,\Omega$, which then requires a load $Z_A = Z_{0,A}^2/R_{OPT,AUX} = 25.0\,\Omega$. As Z_A is forced by the output capacitance of the auxiliary an additional matching network is required to reach Z_{CN}. Additionally, the output matching of the auxiliary must be non-inverting for the Doherty to operate correctly, therefore another impedance inverter, this time made with a quarter-wave transmission line, is added. The impedance of the latter is chosen so that the impedance observed at the common node by the main, which will be modulated at $1.5Z_{CN}$, is transformed to Z_A.

This completes the theoretical Doherty combiner, which will work ideally at the frequency ω_0 and gives a solid reference to take the design forward. However, to design with real device models over a significant bandwidths, it is necessary to keep an eye on the transistors loading and performance in a large signal simulation environment.

4 Keysight ADS Design Template

4.1 Top Level Testbench

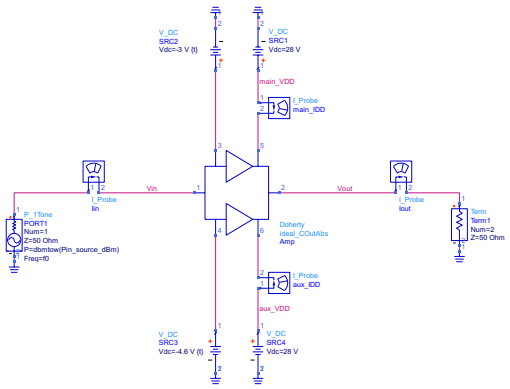


Figure 8: Top level testbench in Keysight Pathwave ADS

Keysight's ADS Pathwave software provides an environment which supports simulation of the Doherty circuit from simple and ideal AC models through full 2.5 or 3D electromagnetic simulation. A top level testbench schematic, shown in Figure 8 provides a consistent set of stimuli, bias voltages, and measurement of the output waveform. These define the interface between the amplifier circuit and exterior components making it a natural boundary. ADS has the ability for a single design "cell" to have multiple variations of the design defined, whether schematics, layouts, or EM models. We use this feature to create a generic Doherty cell which holds the variations at each stage of the design process. Finally the testbench also is linked with the primary Data Display which calculates and plots the key Doherty properties and parameters defined in previous sections.

The top level testbench contains an S-Parameter simulation for stability and basic circuit properties such as input match and small signal gain. This simulation is useful as it provides quick validation of these values, but is limited in the level of detail which its outputs can be used to examine the Doherty behavior. A harmonic balance simulation with swept frequency and input power is the primary tool used to excercise the design. Defining the simulations and the order of the sweeps in this singular top-level testbench makes the test data directly comparable between design stages, simplifying the investigation of changes in performance between steps.

Simple, high-level measurements are defined and calculated by the top-level testbench including P_{out},

P_{in}, P_{DC}, transducer and power gains, DC-to-RF drain efficiency and Power-Added Efficiency based on the voltage and current probes at this level.

4.2 Circuit Probes

The Doherty circuit itself is held in an ADS cell with ports to connect gate and drain supplies, an input for the stimulus signal, and an output of the amplified signal. Probes are inserted inside of the circuit schematic of the amplifier to non-invasively monitor currents and voltages throughout the design.

The input matching networks for a Doherty amplifier largely are identical to those of conventional, single-device amplifiers so are not explored in this paper. The design template however does include probes to measure the input impedance before the power divider, the power division ratio of the input signal to the Main and Auxiliary devices, the input impedances after the divider, and the input impedances at the gate terminal of each transistor. By using current and voltage waveforms these values can be calculated and used during the harmonic balance simulation and directly related to the behaviors analyzed in-depth for the output networks and overall amplifier. Using values from the S-Parameter simulations was initially explored, but improved overall performance and clarity on the causes of changes in performance after each design step was obtained by having the additional information from the power sweep and ease of access to the harmonic content of the waveforms.

The output matching networks contain the majority of the complexity in the Doherty Architecture. Despite that, only a few probe points provide sufficient information to derive all of the metrics discussed previously and to create expressive plots to monitor them. In Figure 9 we can note pairs of voltage and current probes for the Main, Auxiliary, and output paths of the common combining node. The Wolfspeed Modelithics device models expose internal probe nodes for the intrinsic current generator current and voltages, but if these were not present in the model pairs of probes could be added after de-embedding the output parasitics using standard techniques such as Cold-FET bias extraction [2]. For this specific design two additional probe points were added: one between the two auxiliary inverters and another between the two stages of the output matching network.

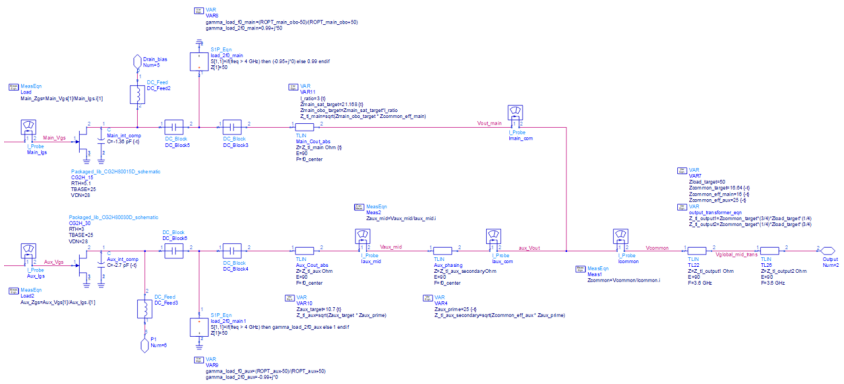


Figure 9: Ideal transmission line implementation of a Doherty with parasitic based inverters

From these measurements the impedances and phase relationships between different points in the output network can be calculated and their behavior shown over frequency and power level. The testbench Data Display formats this information into several plots emphasising different aspects of the Doherty behavior.

4.3 Data Displays

The motivation for the Doherty architecture revolves around using load-modulation to maximize the voltage swing of the Main amplifier at a point backed off from full power, and then extracting additional current at that voltage level by modulating the effective load to a lower value as the input signal level continues to rise. Loadline plots display this behavior most directly by combining the DCIV data measured at the start of the design processes with the intrinsic plane current and voltage waveforms of the simulated signal. Figure 10 shows this data for amplifier simulated just at the back-off point. In the interactive Data Display sliders allow a stimulus frequency and power level to be selected to drive the data plots. The red trace shows the dynamic behavior of the waveform, with the Main transistor just reaching the knee voltage while sourcing a current of $1/3I_{max}$ and the Auxiliary amplifier not yet conducting current. The thin blue trace shows the load-line over the entire range of the power sweep, showing the behavior seen in Figure 3.

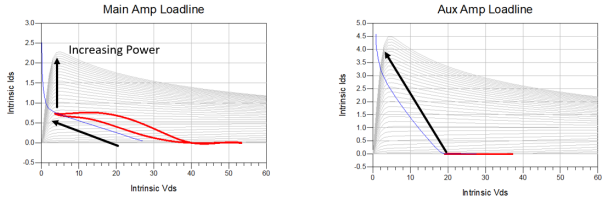


Figure 10: Load lines at the intrinsic generator planes

This data can alternatively be shown as the effective load impedances presented to the transistors at the fundamental frequency. Figure 11 displays the real value of the loads as well as their complex values on a Smith chart. The real-valued chart provides quick access to the load values without distortion of the Smith chart's log based grid and immediate access to the loads at any given source power level. This is highly useful during tuning of the characteristic impedances of the inverters as the match at both backoff and peak power is visible. Issues of insufficient load modulation are immediately apparent as well as errors in the acheived loads. The calculated ideal loads are noted by markers and in this figure it can be seen that the Main's load reaches it's target neither at backoff or saturation. Also the Main amplifier's load is capacitive at maximum power, a deviation from ideal theory which produced marked improvements in efficiency. Possibly this is due to incomplete de-embedding of parasitics in the model.

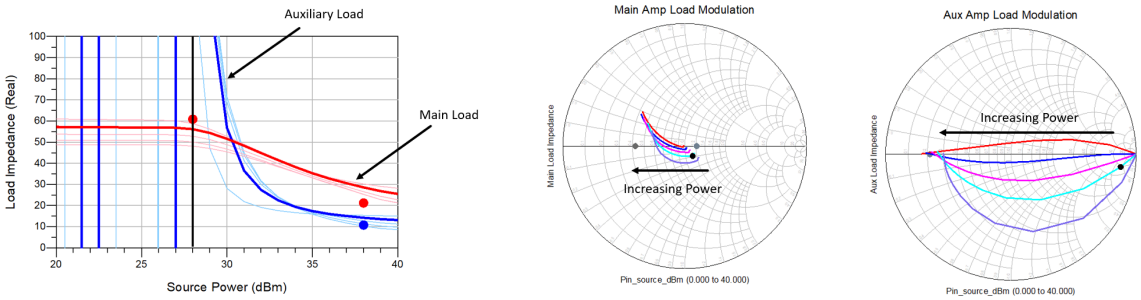


Figure 11: Load Modulation at the intrinsic generator planes

The intrinsic currents and voltages are compared in Figure 12. The template includes plots for both normalized and absolute values. In this case-study the normalized plot of currents shows that at this frequency the Auxiliary is falling just short of supplying two times the Main's current, thus contributing to the under-modulation of the Main's load at saturation as seen in the previous figure. These plots provide a view to the turn-on behavior of the auxiliary allowing the gate bias voltage and input power divider to be tuned such that the Auxiliary begins providing notable current at the OBO power level. Additionally the plots provide a perspective into the saturation behavior of the transistors. In this case the Main transistors voltage does not level off sharply at the OBO point and instead continues to increase into soft saturation in the knee region.

The previous displays relate to behavioral aspects of the Doherty amplifier and without additional

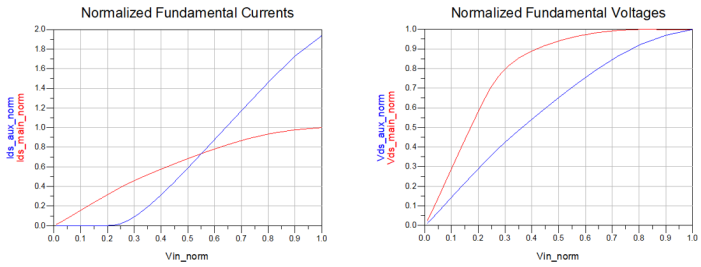
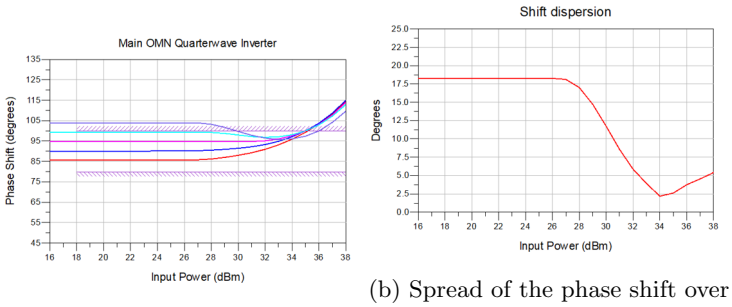


Figure 12: Current and Voltage magnitudes at ω_0

information the designer may not know what circuit component is leading to a deviation from the ideal target performance. Figure 14 shows one of several plots tracking the implementation of the impedance inverters. In this case the Main transistor's inverter, implemented using the technique described in Section 3.3, achieves the 90° phase shift only at the frequency marked in blue, and overall is not centered on the simulated band. The effective load transformation of the inverter will vary as the phase shift changes with frequency so both the absolute value of the shift and the relative range of the shift are useful in optimizing the performance of the real circuit as the non-idealities of the transistors and circuit elements accumulate as the design moves from ideal to layout.



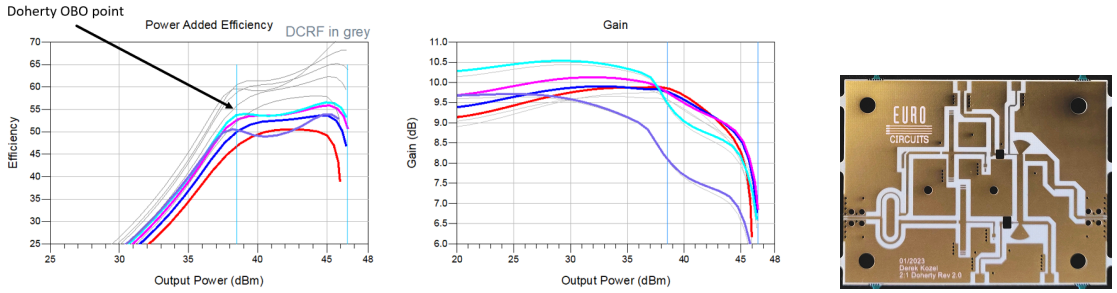
(a) Absolute phase shift

(b) Spread of the phase shift over frequency

Figure 13: Main OMN Inverter

4.4 Performance

The design template also includes a section with common overall performance information such as efficiency, gain, and output power. Figure 14a shows the significant efficiency boost at backoff that a Doherty provides, acheiving nearly 55% PAE at 8.5 dB backoff. Additional plots include stability factor, saturation, and



(a) Simulated performance

(b) Manufactured PCB

Figure 14: Final Design

5 Conclusion

The design template includes over two dozen plots which present both a broad overview of the amplifier's behavior as well as specific, key values particular to the Doherty architecture. Visualizing a consistent set of parameters and metrics throughout the design process, from ideal elements to EM analysed PCB, improves the mapping of theory to final behavior and increases designer visibility into the causes of nuanced interactions. The design template is flexible to other target specifications and extensible to include other design techniques. By acknowledging the inevitable non-ideal nature of the devices and circuits in a real application the template enables designers to apply their domain knowledge and techniques with the aid of pre-configured testbenchs and measurement displays. Future work will provide an example with packaged devices and add additional measurements as optional extensions to the template to increase it's utility in power amplifier system design.

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