Designing Calibration Standards for Cryogenic On-wafer S-parameter Measurements

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Abstract

Microwave on-wafer measurement at cryogenic temperature plays an important role in the development of planar circuits for quantum computers. Such measurements enable direct characterisation of quantum circuits, without the need for additional components such as chip-to-PCB wire bonds, coaxial connectors, attenuators and cables. At NPL, we have developed a bespoke calibration substrate for cryogenic on-wafer measurements at temperatures down to 4 kelvin (K). High-resistivity silicon and niobium were used as the substrate and metallization material, respectively. The niobium metal layer is expected to be superconducting at approximately 9 K, making it an ideal choice for fabricating standards for use with our 4 K cryogenic probe station. This paper describes the design process and preliminary study of the calibration substrate based on full-wave electromagnetic (EM) simulations using ANSYS High-Frequency Structure Simulator (HFSS).

1 | INTRODUCTION

Even in room temperature environments, adverse effects due to cables, connectors and wire-bonds significantly reduce S-parameter measurement accuracy. These adverse effects become more significant and unpredictable at cryogenic temperatures. Appropriate calibration needs to be employed to reduce these effects and shift the calibration reference planes as close to the device under test (DUT) as possible. Calibration kits based on printed circuit boards (PCB) have been developed, which allow for calibration planes to be shifted to the quantum RF integrated circuit (RFIC) [1,2]. These PCB based systems allow unwanted components between the reference planes and the vector network analyzer (VNA) ports to be de-embedded, facilitating more accurate measurements. However, whilst this allows accurate characterization of the chip-level system, measurements are still heavily influenced by components such as wire bonds and co-planar waveguide (CPW) feedlines.

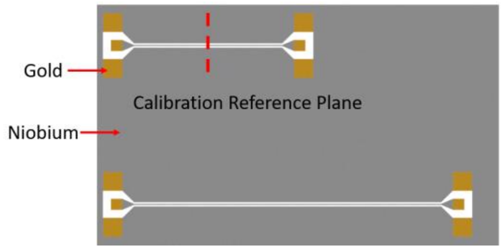
On-wafer level calibrations allow for the reference planes to be positioned as close to the DUTs as possible, whilst also eliminating the need for components such as switches and bonding wires. For accurate cryogenic on-wafer calibrations, having well-designed calibration standards is crucial. A typical cryogenic on-wafer measurement environment introduces many challenges, originating from factors such as limited space, visibility and probe movements. Therefore, ideally, the number and sizes of the calibration standards need to be as small as possible. In this paper, we present preliminary findings from the development process for a calibration substrate that can accommodate multiple different types of standards for calibration schemes such as Thru-Reflect-Line (TRL) [3] and multi-line TRL [4]. The purpose of this calibration substrate is for us to explore behaviours of superconducting on-chip calibration standards and find the best strategies for achieving accurate calibrations and measurements while using the minimum number of standards.

2 | CALIBRATION STANDARDS

Various CPW calibration standards are employed to support conventional single-line TRL, and multi-line TRL calibration schemes. Compared to other calibration schemes such as Short-Open-Load-Thru (SOLT) [5] and Line-Reflect-Match (LRM) [6], TRL calibration does not require the standards to be accurately defined [7]. Also, TRL relies on lines; changes in length of these lines does not significantly affect the calibration accuracy. No resistive load is involved, and therefore these standards are relatively easy to fabricate.

The substrate has a thru, a set of seven different length line standards and a set of reflect standards (shorts and opens), allowing for wide frequency band coverage up to 20 GHz. Illustrations of some standards are shown in Fig.1.

Each standard consists of two parts: a contact pad and a main transmission line. Due to the dimensional restrictions of quantum devices, the main structure of the CPW is relatively small and therefore too small for RF probes to land. Therefore, each port of the standards is designed to have a larger area (150 μm pitch) for RF probes to make contact. As can be seen from the diagram of the thru, all of the standards are designed to have their calibration reference plane offset from the probe tip and landing pad with a section of transmission line between them.



(a)

(b)

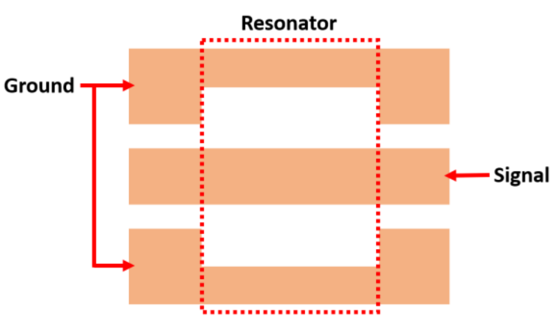
Figure 1: CAD drawing of the calibration standards: (a) Thru, including reference plane indicator (top) and Line (bottom); and (b) Reflect Standards: short (top) and open (bottom).

The calibration standards are patterned on a high-resistivity silicon substrate (nominal thickness: 280 µm, resistivity: 10,000 ohm-cm), which is a typical choice for quantum planar circuit devices. The ground-signal-ground CPW structure is metalized with a thin film of niobium (100 nm thick) which is expected to be superconducting at and below 9.3 K [8]. The contact pads are reinforced with a layer of gold patches to protect the niobium layer from multiple probe contacts. On Fig. 1 the niobium metallization and gold pads are shaded with grey and yellow, respectively.

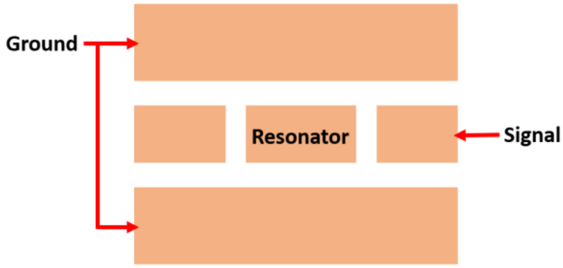
3 | VERIFICATION DEVICES

Two sets of verification devices, a Beatty line, and a weakly coupled resonator are included on the calibration substrate and are intended to be used to verify the calibration and to extract characteristics of the transmission line.

A typical Beatty line is a transmission line with stepped characteristic impedance planes, as shown in Fig. 2(a). The highly resonant nature of the Beatty line produces a wide range of S-parameter responses, making it a good choice for a verification device [9].



(a)



(b)

Figure 2: Illustration of the verification devices: (a) Beatty line; and (b) weakly coupled resonator.

As illustrated in Fig. 2(b), a weakly coupled resonator is a capacitively coupled resonator with a very high Q-factor at a given frequency. This behaviour can be utilized to determine the transmission line's characteristics, such as the substrate's dielectric constant.

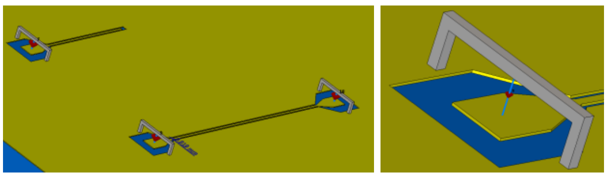
The length of the resonator is tuned using full-wave EM simulation, and this will be discussed in the next section. CAD drawings of the verification standards are shown in Fig. 3.

Figure 3: CAD drawing of the verification devices: a Beatty line (top) and a weakly coupled resonator (bottom).

4 | EM SIMULATION

Full-wave EM simulations were employed, using ANSYS High Frequency Structure Simulator (HFSS) The simulation was conducted to determine the minimum required distance between the standards that ensure no cross-coupling between them and to tune the resonator lengths of the verification devices.

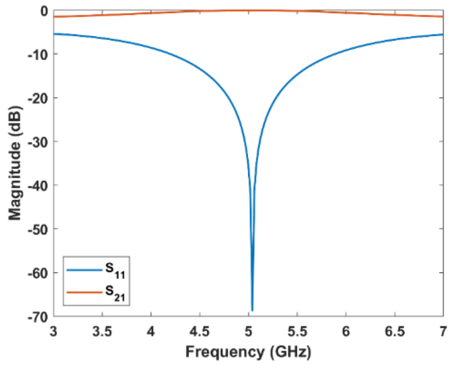
Since we plan to test the substrate at 4 K, below niobium's superconducting transition temperature, a perfect electric conductor (PEC) was used to model the niobium layer [10]. Also, as we wanted to simulate the effects of having contact pads to CPW transitions, lumped ports were used with a PEC ground bridge [11]. The probe landing pad, transition structure and ground bridge for the EM simulation are shown in Fig. 4.



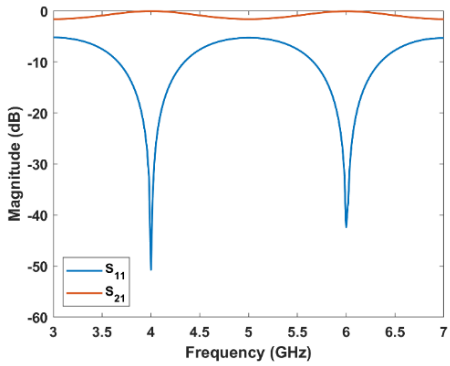
(a) (b)

Figure 4: 3D simulation set up of the calibration standards: (a) short (top) and thru (bottom) standards; and (b) zoomed in view for the port excitation.

For both Beatty lines and the weakly coupled resonators, parametric analysis was done to vary the length of the resonators to fine-tune the frequency responses. The operational frequency range of the devices is 3 to 7 GHz. To verify the calibration, having multiple resonances across the whole band is preferable. However, due to limited space on the wafer substrate, two different lengths of Beatty lines were designed. The shorter line is tuned to have a resonance at 5 GHz and the longer one is tuned to have resonances at 4 GHz and 6 GHz. The initial design of a Beatty line and preliminary simulation results are shown in Figs. 5(a) and (b), respectively. The length of the weakly coupled resonator is tuned to have a resonant point at 5 GHz as shown in Fig. 6.



(a)



(b)

Figure 5: HFSS simulation S-parameter results of the Beatty lines: (a) short line; and (b) long line.

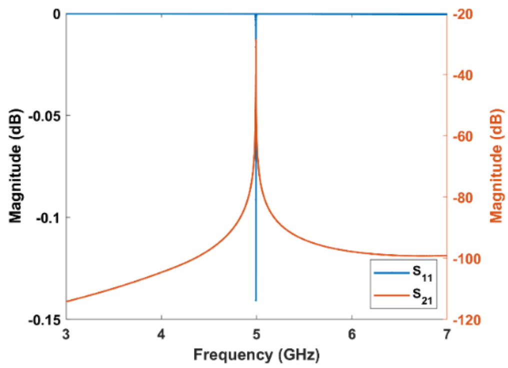


Figure 6: HFSS simulation S-parameter results of the weakly coupled resonator.

5 | MEASUEMENT SET-UP

The measurements will be carried out using a 4 K cryogenic RF probe station which is currently being commissioning. The probe station supports two-port RF measurements and is equipped with standard 2.92 mm coaxial connectors (which can operate up to 40 GHz). There are four micro-controllable probe arms that can accommodate a pair of DC and RF probes. It is fitted with a brass chuck that can fit a standard 4-inch wafer. The whole system is floating on an active pressurized isolator to minimize vibration. The setup is shown in Fig. 7.

(a) (b)

Figure 7: Measurement set-up showing the cryogenic probe station: (a) internal view showing the probe arms and the DUT chuck; and (b) external view.

6 | CONCLUSION & FUTURE WORKS

In this work, we have presented some of the advancements we have made in our current cryogenic on-wafer capability development process. We have developed a bespoke calibration substrate for cryogenic on-wafer measurements at temperatures down to 4 K. High-resistivity silicon and niobium were used as the substrate and metallization material, respectively. A full-wave EM simulation has been utilized to help the design, tuning and verification processes. Various S-parameter calibration standards such as thru, lines and reflects are included on the calibration substrate. Also, Beatty lines and weakly coupled resonators are added for calibration verification and to extract characteristics of the transmission line.

By using the 4 K cryogenic probe station, we will be able to measure all the calibration standards and verification devices at both room temperature and 4 K. We will compare measured results at different temperatures and validate the EM simulation results. By exploring all the possible combinations of the standards, and by characterizing them, we will be able to pick and choose the most appropriate combinations of standards for different application requirements. This will allow the calibration standards on future wafers to occupy minimum space, thus allowing more space for the quantum circuits and devices. This will reduce the DUT fabrication costs while still maintaining the accuracy of the measurements.

AWCKNOWLEDGEMENT

This work was supported by the U.K. Government's Department for Science, Innovation & Technology (DSIT) through the U.K. National Quantum Technologies Programme.

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